**Amendments to the Specification:**

Amend the specification by inserting before the first line the sentence:

This is a continuation of application Serial No. 10/316,166 filed December 10, 2002, which application is hereby incorporated by reference in its entirety.

Please amend the paragraph beginning at page 4, line 13 to page 5, line 9, with the following rewritten paragraph:

~~A non-volatile semiconductor memory device is provided to include a memory cell array having electrically erasable and programmable non-volatile memory cells, a part of the memory cell array being defined as a initial set-up data region for storing a plurality of initial set-up data that define memory operation conditions, data latch circuits for holding the initial set-up data read out from the initial set-up data region, a controller for controlling data program and erase operations for the memory cell array, and a clock generator for generating a clock signal that is used to define an operation timing of the controller, wherein the controller is configured to perform such an initial set-up operation that sequentially reads out the plurality of initial set-up data stored in the initial set-up data region and transfers them to the respective data latch circuits on receipt of power-on or a command input, the initial set-up operation being so performed as to read out a clock cycle adjustment data within the plurality of initial set-up data stored in the initial set-up data region in the beginning, thereby adjusting a clock cycle of the clock signal output from the clock generator by use of the clock cycle adjustment data, and then reads out the remaining initial set-up data by use of the adjusted clock signal.~~

According to an aspect of this invention, there is provided a non-volatile semiconductor memory device, including:

a memory cell array having non-volatile memory cells arranged therein, in which initial set-up data are stored;

data latch circuits configured to hold the initial set-up data read out from the memory cell array;

a controller configured to control operations of the memory cell array; and

a clock generator configured to generate a clock signal that is used to define an operation of the controller, wherein

the controller is so programmed as to read out a clock cycle adjustment data within the initial set-up data in the beginning after power-on, thereby adjusting a clock cycle of the clock signal output from the clock generator by use of the clock cycle adjustment data, and then read out the remaining initial set-up data by use of the adjusted clock signal.